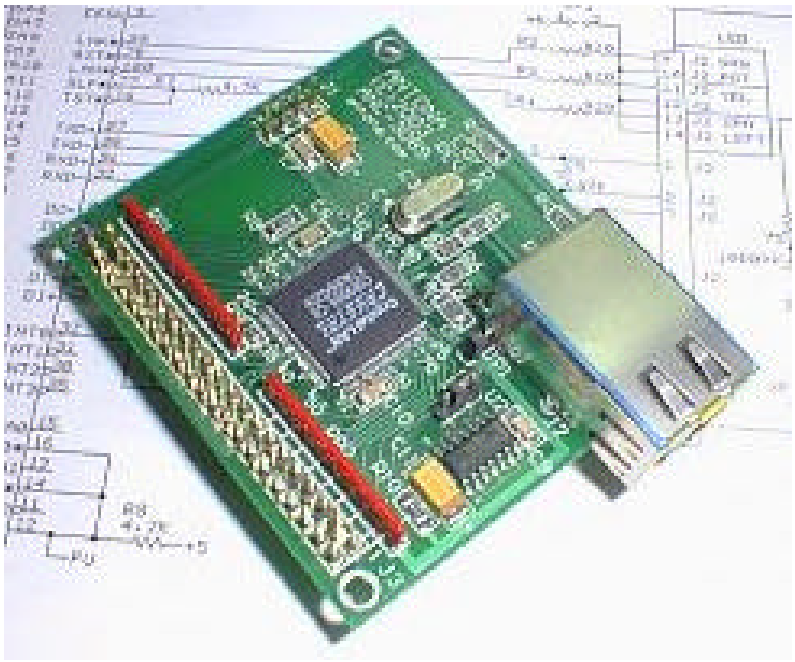
Rev. A
$ 5.00

ANC - 3089
Ethernet Adapter

Antona

Antona Corporation, Los Angeles, CA



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Features

- IEEE-802.3 Ethernet MAC Engine
- 10Base-T Physical Layer digital and analog electronics
- 8-bit or 16-bit interface
- Operates with only 4 address and 4 control lines
- 4K on board RAM buffers transmit and receive frames
- Auto receive polarity correction
- Loopback data for local test mode
- Latest surface mount technology for low power and small size
- 3 Status LEDs for Link, Frame Activity and a User definable indication
- Reset selectable on positive or negative level signal

Overview

The ANC-3089 adapter provides a complete 10Base-T media access control (MAC) ethernet engine "physical layer" electronics for TCP/IP network interface applications. The MAC engine, which formats frame data, calculates CRC, transmits and receives packets of data compatible with the ethernet IEEE 802.3 interface standard. The card interfaces to the outside network world by a shielded RJ-45 ethernet connector. Control of the adapter is through a 40-pin connector which mates with an 40-pin IDC ribbon cable connector, or may be connected to from the solder side of the card via .018 inch gold machine pins or wire wrapped using the .025 inch square wire/wrap post to machine pin connectors included with the adapter. The adapter finds use in equipment prototyping and short production runs. A single +5V DC at 60ma powers the card through a 4-pin SIP connector which can also be attached to from the top or bottom side of the card.

The ANC-3089 adapter is not the world's smallest internet web server. It is the 'physical layer' of an ethernet client. That part of a whole application, which forms the ethernet hardware interface to the outside world. The software which controls the adapter and the user application makes up the complete ethernet enabled system. Using the adapter to interface a chassis mounted video switcher to act on commands received through an in plant ethernet would be an example of how this product was intended to be used.

The designer should download the CS8900A Product Data Sheet, the CS8900A Technical Reference Manual (AN83), the Application Note "CS8900A Frequently Asked Questions" (AN205) and, for 8-bit operation, the Application Note "Using the Crystal CS8900A in 8-Bit Mode" (AN181) from the Cirrus Semiconductor website (www.cirrus.com). Use the search function on their homepage with 'CS8900A'. The operation of the ANC-3089 adapter *is* the CS8900A ethernet chip. The following pages detail specific features of the adapter board, and general information on the ethernet chip that is covered in detail by the documents above. The book "TCP/IP Illustrated, Volume 1 – the Protocols" by Richard Stevens, published by Addison Wesley (ISBN 0201633469) was a valuable source of information on how ethernet messages are generated and read in various protocols. There are websites offering partial or complete TCP/IP stacks (software protocols that run under TCP or UDP) for the CS8900A for several different processors. Lastly, there are thousands of pages of "RFC" (request for comment) numbered documents on the internet detailing every aspect of protocol operation, some of which may also be useful. There is no shortage of "RFC" protocol

information, indeed the opposite seems to be the case – too much information to shift through to find what is needed. Doing a search with one of the major search engines will produce several useful resources. It is the author's hope that the following pages will save the designer a few hours time in learning how to use the adapter to interface with an ethernet.

Mechanical Specifications

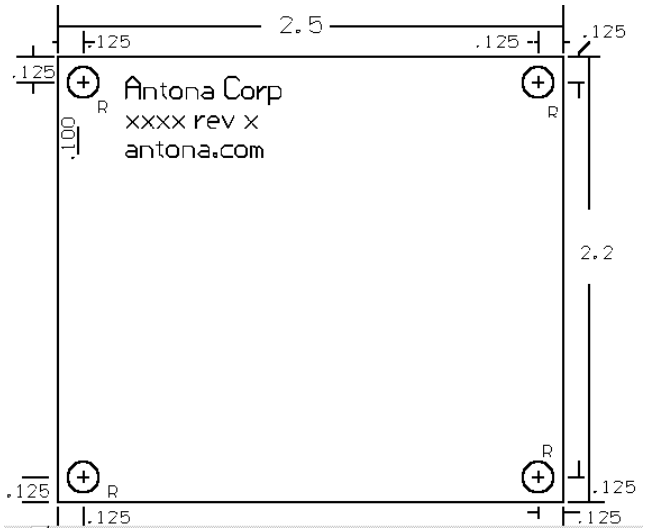

Figure 1 – Adapter Mounting Detail

Adapter size: 2.5"W X 2.2"L X 0.7"H

Connectors: Digital interface - 40-pin IDC on top side of PCB, 0.018" dia. Machine pins on bottom side
Power - 4-pin SIP type connector as above
Ethernet - Transformer isolated shielded 8-pin RJ-45

Electrical Specifications

Power requirements = 5v DC at 60 ma maximum
Ethernet output drive = 100 ohm impedance, meets IEEE-802.3 specification

Adapter Installation

Turn off any and all power supplies to the attached equipment before installing or removing the adapter. ***Never install or remove the adapter with the power applied to any of the attached equipment. This could result in permanent damage to the adapter due to static discharge.***

The adapter may be mounted on a second PCB or prototyping perf board when wire wrapping is used. The designer can also use an IDC ribbon cable plugged into the top side of the ANC-3089 and then translate the required data, address and control signals to and from the target processor board. ***Be sure to look at the pin 1 identification on the adapter to insure that the proper connector polarity is observed***. The ANC-3089 has 4 mounting holes at each corner of the card for #6-32 bolts to use for permanent installations to assure good long-term connection.

If you are using the adapter with a 40-pin ribbon cable on J3, the ribbon cable should not exceed 3 feet .

Powering

The adapter power is attached to J1, a 4-pin SIP (single inline package) type 0.1" pin-to-pin spaced connector. Only 2 of the pins are needed for powering the adapter card with an external +5V DC power source. The table "Connections to the ANC-3089" shows which pins are used for the external source of DC to power the adapter.

Adapter Options and Features

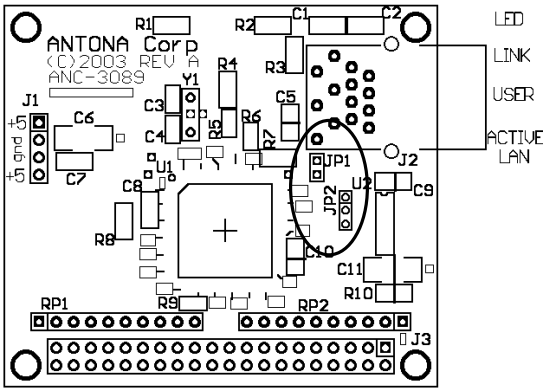

Figure 2 - ANC-3089 jumper locations

Jumper Options

When shipped, the ANC-3089 is set for a negative going pulse to reset (JP1) the adapter and the LEDs are enabled (JP2). Any references to 'horizontal' and 'vertical' below are in respect to figure 2 above. The schematic gives another view of each jumper showing the settings on isolated block drawings of each jumper function.

LED Enable - JP1

The LEDs on the adapter card are handy for product development, troubleshooting and customer service calls. They can provide an immediate indication of network connection, packet transmit / receive and a user selected function for alarm or process state. In some applications where the LEDs are not easily viewable, or portable applications where power is limited, it may be desirable to disable the LEDs. Removing the vertical shunt across JP1 located just below the RJ-45 connector, will disable the LEDs.

Reset Signal Polarity Select - JP2

Depending upon the processor used with the ANC-3089, there may be a positive or negative going reset pulse available to the designer to work with. The reset signal can also be generated using a digital signal controlled by the target processor. Being able to generate a hardware reset to the CS8900A is useful if the chip appears to have stopped operating correctly. When shipped, the card is configured for a normally high, negative pulse reset signal with the shunt over the lower 2 pins of the JP2 jumper. Putting the shunt over the upper 2 pins

configures the card to accept a normally low, positive pulse. This is common for the 8051 family of microprocessors. The vertical 3-pin jumper is located just to the left of U2 on the circuit board.

LED Indicators

Built into the RJ-45 connector are three LEDs that can be set up in a variety of ways. The right most green LED indicates when a network 'link' is recognized and remains on as long as a network connection is maintained. The middle yellow LED is a user definable indicator set under software control of the application program. The right most green LED indicates when a new packet has arrived, been transmitted or a collision has occurred by 'winking' on for 6 ms. The LED functions are listed on the right hand side of figure 2 above.

Processor and Power Connection

Power Supply

SIP Pin #	*Function*	*Comment*	*Data Direction*
1	Primary +power	+5 V DC	input to adapter
2	Primary ground	Ground	input to adapter
3	Secondary ground	Ground	input to adapter
4	Secondary +power	+5 V DC	input to adapter

Connect the +5v DC power to pin 1 and the mating power supply ground to pin 2 of J1. Only 2 pins are needed to power the adapter, the other 2 secondary pins are not needed on the current PCB design.

Ethernet Connection

The RJ-45 connector, J2, provides the actual connection to the ethernet. The pinouts from the connector are standard and should interface with CAT-5 cable mated with 8-pin RJ-45 male connectors wired for ethernet use. Note pin 6 is RC-, not pin 4 and that pin 4 is shorted to pin 5 and pin 7 is shorted to pin 8.

RJ-45 pin #	*Function*	*Comment*	*Data Direction*
1	TX+	Transmit plus	Output from adapter
2	TX-	Transmit minus	Output from adapter
3	RC+	Receive plus	Input to adapter
4		Shorted to pin 5	See schematic
5			
6	RC-	Receive minus	Input to adapter
7		Shorted to pin 8	See schematic
8			

Processor Interface

Hardware Wiring

The 40-pin connector J3 is the interface between the ANC-3089 ethernet card and the designer's microprocessor, microcontroller or DSP chip. To ease this process, and offer a universal way to connect to the card, there are 3 ways the adapter may be interfaced. By using a standard 40-pin IDC ribbon cable, the user can connect to the card in applications where the ANC-3089 is mounted separate from the target processor controlling it. An example would be where the adapter is mounted within a piece of equipment with the RJ-45 connector sticking out of the back to access the ethernet. For prototyping, J3 can also be accessed on the opposite side of the PCB for applications where a daughter board arrangement is preferred. The bottom side 0.018" diameter machine pins plug into standard 0.1" center-to-center component sockets or mating machine pin sockets. Lastly, we have included wire wrap posts for both J1 and J3 to use in wire wrapping prototypes of initial designs.

Data and Control

The ANC-3089 adapter can be viewed as a 40-pin peripheral chip. The Cirrus CS8900A ethernet chip is addressed as eight 16-bit memory mapped registers. The designer needs to generate a negative-true chip select to pin 17 (AEN) and suitable negative-true read/write memory signals. The table below shows the pinouts of the 40-pin connector and figure 3 below is a physical map of the pin connections. Be aware of the timing for the data, address and read/write signal to insure the processor you are using generates signals conforming with the minimums and maximums needed by the CS8900A for reliable operation.

8-Bit Mode

For minimum interfacing with an 8-bit processor, 16 signal lines for data and control are required. The 8 data lines (D0-D7), 4 address lines (A0-A3), plus the reset, chip select (AEN), write data (WR*) and read data (RD*) control the adapter operation. Reading or writing to the 16-bit registers is performed 8-bits at a time loading an upper and lower byte to form the 16-bits used internally by the CS8900A. *Note that the byte order that data is written or read to/from the CS8900A is important and depends upon if data or control information is being processed. Check with the appropriate application note from Cirrus detailing 8-bit operation (AN181) for how this is done*. Interrupts are not usable in 8-bit mode so the designer should poll the CS8900A for complete frames. There is 2K worth of input buffer space, so while a frame is being processed, additional frames can be input without interruption. If *every* packet was input on a network with heavy traffic, the processor would probably not be able to keep up - with or without an interrupt signaling that a new frame had arrived. Filtering and disabling the 'promiscousA' bit of Receive Control Register (104H) will limit the number of frames stored to the on board RAM buffer to those frames being directed to the individual MAC address of the adapter. The Receiver Event Register (4H) has a 'IndividualAdr' bit which can be tested to identify frames sent to the adapter's MAC also. See Appendix B which shows a typical 8-bit interface for the 8051 family of processors.

16-Bit Mode

For 16-bit applications, connect SBHE* (pin 23) to AEN (pin 17). The toggling of the SBHE* line is what signals the CS8900A chip to use the upper 8-bits in addition to the lower 8-bits for data and control operation. In addition to the address and control lines detailed above all of the 16 data lines (D0-D15) are connected to the processor. In 16-bit operation, an interrupt can be set up to signal frame activity on pin-26 (INTR).

Data and Control Signals

pin # (J2)	FUNCTION	Comment	pin # (J2)	FUNCTION	Comment
1	D7	MSB of 8-bit data bus	2	Reset	Reset pulse neg/pos
3	D6		4	Ground	Digital ground
5	D5		6	Ground	
7	D4		8	Ground	
9	D3		10	Ground	
11	D2		12	Ground	
13	D1		14	Ground	
15	D0	LSB of 8-bit data bus	16	Ground	
17	AEN	Chip select - neg	18	A3	MSB Address line
19	WR*	Write data pulse – neg	20	A2	
21	RD*	Read data pulse – neg	22	A1	
23	SBHE*	8 or 16-bit operation	24	A0	LSB Address line
25	D8	LSB of upper byte	26	Interrupt	Interrupt (16-bit use)
27	D9		28	Ground	
29	D10		30	Ground	
31	D11		32	Ground	
33	D12		34	Ground	
35	D13		36	Ground	
37	D14		38	Ground	
39	D15	MSB of 16-bit bus	40	Ground	

neg = negative true logic (logic low to enable function)

Data/Control Signal Map

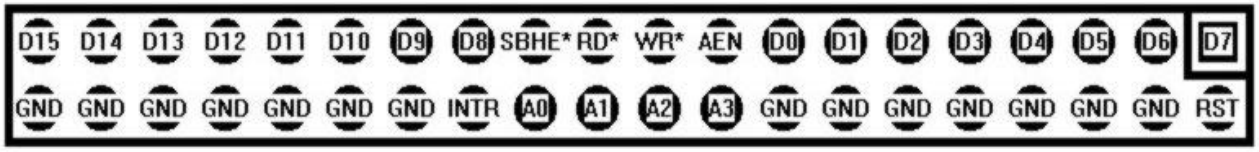

figure 3 – J3 Data and Control Map

The connector map above is useful in quickly identifying the pinouts on the 40-pin processor interface. Only 16 pins are needed to interface an 8-bit processor to the ethernet. When a 40-pin ribbon cable is used, there is a ground pin placed between most of the data lines to provide faraday shielding.

Adapter Operation

Addressing

The logical card address detailed in the CS8900A documentation refers to the default address range of 300H to 30FH to control the operation of the chip. The adapter is hard wired to the base address 300H to match the power up default of the CS8900A chip. The physical address of the ANC-3089 adapter is controlled by the user to be decoded by using the AEN as a low logic chip select and

the A0 to A3 lines to form the lower 4-bits of the address. The adapter can be driven as an I/O or memory mapped peripheral. Referring to Appendix B, the schematic shows the adapter being decoded by inverting the A15 line as a chip select, and using the A8 to A11 lines from the 8052 processor to drive the A0 to A3 adapter lines. This example provides a simple interface requiring a minimum of external circuitry to map the logical 300H-30FH range to the physical 8000H-8F00H in the 8052's memory space.

Software

The adapter is really a special purpose embedded processor that is equipped with the analog and digital circuitry needed to physically connect with the ethernet, an IEEE-802.3 MAC engine and external processor interface. The ethernet packets processed by the CS8900A are formatted frames written and read from the processor interface. The ethernet adapter does not know the information content of the frames, only that they have been input through the ethernet interface, or transferred from the processor connected to the 40-pin connector for transmission. It is up to the processor running the ANC-3089 to input, check and decode the incoming frames and generate the proper ethernet frame output messages (called datagrams in ethernet-speak). Like most other microprocessor or microcontroller peripheral chips, the ANC-3089 needs to be initialized after power up for the desired mode of operation and then, as appropriate, act on or control the end application. For more detailed software operation, refer to the documents listed under the Overview section on page 3.

The ethernet software required is a function of the user end application. An example would be to use the card in a system that monitors some analog condition (like temperature), and then send an email to a preset email address when a upper or lower limit is exceeded. In such an application SMTP, a common email protocol, would be coded by the programmer to generate and send out mail datagrams over the ethernet interface to a locally connected IP address, or a gateway to the internet to be transmitted anywhere in the world. Another example is using the adapter to interface to a computer driven telescope. Here the designer would probably use User Defined Protocol (UDP) to send commands to the telescope for object selection and receive JPEG images back from the telescope's eyepiece mounted CCD camera.

Appendix A – Troubleshooting Guide

Ethernet Interfaces

Here are some common sources of problems and tests you can make to diagnose your ethernet interface. Application Note – AP205 from Cirrus (cirrus.com) should also be downloaded and looked over.

Powering

Be sure that the +5v DC power is being applied to the card. The right-hand side green 'LINK' LED should be on even if there is no ethernet data or software running on the adapter card if either a loopback or ethernet cable is connected to the on board RJ-45 connector.

Interface Wiring

Check that all of the processor to adapter signal wires are connected correctly. A missing connection and/or a miswired connection is a common mistake. If is somewhat harder to do, but connections can be shorted also. Any of the above will cause the adapter to appear not to work at all.

Loopback Test

Without having an external network running, the designer can use a loopback test using a short RJ-45 cable with the TX+ connected to the RC+ and the TX- to the RC-. Initialize the CS8900A chip for ''promiscousA' mode and "full duplex" operation so that any frame transmitted will be received and read in. Then generate a transmission and check the received message. Using an in-circuit emulator to replace the processor being interfaced with the adapter will speed up the process. If you are able to read a loopback transmission, the adapter is working.

CABLING

On the RJ-45 connector the right-hand side green 'link' LED should be on if the cable going from the RJ-45 is connected to an ethernet signal source, like a hub. The other green 'frame activity' LED on the left-hand side of the RJ-45 will wink on for 6ms when a frame is received or transmitted. Even if the CS8900A chip is not initialized and just powered up, those 2 LEDs should function as described.

If one of the interface wires used is not connected (open) or shorted to another wire, the whole interface will appear not to be working. Try using another cable or the loopback test described above through the cable to verify operation. If you can not get the loopback test to work through the cable, it will not work in your application. Even cables purchased with molded ends can be damaged or, as described in the next sentence, not wired right.

The cable wiring should use twisted pairs of wires for transmit on pins 1 and 2 while the receive pair is pin 3 and 6 (not pin 4). Be sure to verify that any purchased cables follow that wiring, many do not.

Jumpers – RESET and LED Enable

Make sure that jumper 2 is set so that the signal being applied to the ethernet chip 'RESET' is normally low. If it is being held high, the ethernet chip will not operate.

If none of the LEDs work, check that JP1 has a shunt across the two pins enabling power to the LEDs.

Program Operation

The ethernet adapter handles the transmitted and received frames, but the processor must interpret and generate the data as the ethernet chip has no idea of the actual frame content or meaning. Make sure the CS8900A is being initialized properly for the mode of operation you intended and that data being sent and received is properly formatted for the protocol you are working with. *If the program is not setup right, the adapter will appear not to be working at all*.

Chip Timing

Be aware of the timing for the data, address and read/write signal to insure the processor you are using generates signals conforming with the minimums and maximums needed by the CS8900A for reliable operation. A fast 8051 processor may be generating a RD* or WR* signal that is too short for the CS8900A to act on. Such timing problems can be solved by generating the control signals in software rather than using the hardware signals of the processor.

Now What?

If none of the above seems to fix the problem, but both green LEDs are working as described above in the “CABLING” heading, the adapter is probably working and you may now need to examine and monitor the signals with an oscilloscope and use an ethernet frame analysis software tool to examine the transmitted and received ethernet data packets. Each adapter is tested before shipping on a PC with an ethernet interface card running through a hub connected to a 40’ CAT-5 cable. Like everything, occasionally an adapter can go bad because they are damaged in shipping or infant component burnout. We do warranty our adapters, so if it still does not work, call Antona and we will work out an adapter exchange.

Appendix B – 8052 Interface Example

Here is an example showing how to interface an 8052 microcontroller with the ANC-3089 ethernet adapter.

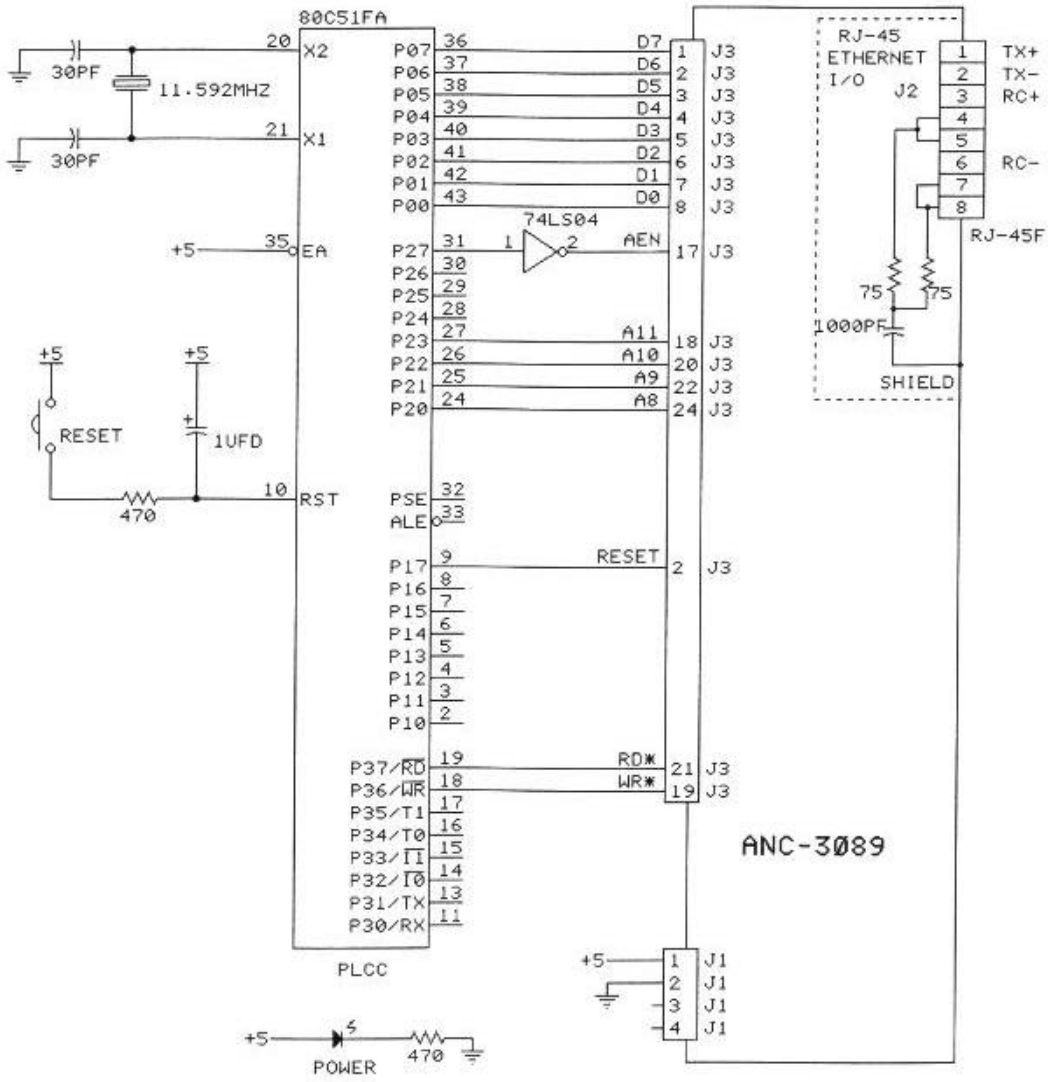

figure 4 – 8052 interface example

The adapter is addressed as external memory beginning at location 8000H and uses the 8052's A8-A11 address lines to control the adapter's A0-A3 address lines for directing control and data to the CS8900A registers. This uses a single section of a 74LS04 to invert the A15 line from P2.7 of the 8052 pictured above. The designer could use P1.6 as a chip select clearing then setting the bit when I/O is being performed to the adapter and do away with the added inverter. This simple minded interface allows 3 more memory mapped peripherals to be added (useful for making the system actually *do* something) by using the A12, A13 and A14 (P2.4, P2.5, P2.6) address lines on the 8052 as additional chip selects. P1.7 is used as a software controlled reset line to the CS8900A and P3.6 / P3.7 furnish the respective write and read signals *If higher speed processors are being used, it may be necessary to drive the write*

and read signals with software generated pulses because the CS8900A requires a minimum pulse width of 135ns.

Appendix C -Circuit Board Schematic

The following page contains the schematic for the 3089 adapter. The schematic and card artwork are copyright protected by Antona Corporation and are included only to aid the end user to configure the adapter or for competent technical service personnel to use in maintenance or repair.

Note: The schematic is included with the purchase of the product.